



Attorney's Docket No.: 104F-120001 / F51-143214M/TOM

2825
#5/A
ZBB
11-6-03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Yoshinori Hino et al. Art Unit : 2825
Serial No. : 10/080,823 Examiner : Phallaka Kik
Filed : February 21, 2002
Title : PATTERN LAYOUT METHOD OF SEMICONDUCTOR DEVICE

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT IN REPLY TO ACTION OF AUGUST 1, 2003

Please amend the above-identified application as follows:

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CERTIFICATE OF MAILING BY FIRST CLASS MAIL

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage on the date indicated below and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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